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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/825,946	04/05/2001	Junji Noguchi	501.39932X00	5570

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ANTONELLI TERRY STOUT AND KRAUS
SUITE 1800
1300 NORTH SEVENTEENTH STREET
ARLINGTON, VA 22209

EXAMINER

VU, HUNG K

ART UNIT PAPER NUMBER

2811

DATE MAILED: 11/20/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/825,946

Applicant(s)

NOGUCHI ET AL.

Examiner

Hung K. Vu

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 22 August 2002.
- 2a) ☒ This action is FINAL. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-35, 37, 38 and 42-45 is/are pending in the application.
- 4a) Of the above claim(s) 1-19 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 20-35, 37, 38 and 42-45 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 9. 6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 20, 28-35, 37-38 and 42-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Edelstein et al. (PN 6,181,012) in view of Nogami et al. (PN 6,242,349).

Edelstein et al. discloses, as shown in Figure 2 and 4D, a method of fabricating a semiconductor integrated circuit device comprising,

- providing a semiconductor substrate (52) having a first main surface,
- forming a first insulating film (54) over the first main surface of the semiconductor substrate,
- forming an embedded interconnection slot over the first insulating film main surface,
- forming a connecting hole in a bottom surface of the embedded interconnection slot, and connected to a lower conducting layer (46),
- forming a conducting barrier film (72) over surface region of the bottom surface and side surface of the embedded interconnection slot and the connecting hole,
- forming an embedded metal interconnection layer (56) having copper as its main component embedded in the interconnection slot and in the connecting hole in which the conducting barrier film is formed,

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forming a cap insulating film (silicon nitride, 101) so as to cover the embedded metal interconnection layer and the upper surface of the first insulating film, wherein,

the concentration of components other than copper in the embedded metal interconnection layer in the finished semiconductor integrated circuit device does not exceed 0.8At% (0.001 wt% C), and

the film thickness of the thinnest part of the conducting barrier film in the side walls of the embedded interconnection slot and the connecting hole is about 10nm.

Edelstein et al. does not disclose the thickness of the conducting barrier film is less than 10nm. However, Nogami et al. discloses an integrated circuit device having the conducting barrier film with the thickness between 5nm to about 150nm. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the conducting barrier film of Edelstein et al. having the thickness of less than 10nm, such as taught by Nogami et al. in order to reduce the contact resistance and to improve the circuit performance.

With regard to claim 28, Edelstein et al. and Nogami et al. disclose performing the CMP to the first metal film. Maekawa does not disclose the CMP is abrasive particle-free CMP. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to perform the abrasive particle-free CMP in order to prevent the surface damage to the first insulating film.

With regard to claims 29-31, although Edelstein et al. and Nogami et al. do not teach exact the mass ratio of abrasive particles, as that claimed by Applicants, however, it would have been

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obvious to one having ordinary skill in the art at the time the invention was made to form the circuit having the desired mass ratio of abrasive particles, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

With regard to Claim 37, Edelstein et al. and Nogami et al. disclose the film thickness of the thinnest part of the conducting barrier film in the side walls of the embedded interconnection slot and the connecting hole is not more than 5nm.

With regard to Claims 38 and 42, Edelstein et al. and Nogami et al. disclose there might be no conducting barrier film. (Note Figure 2 of Nogami et al.)

With regard to Claims 43-45, Edelstein et al. and Nogami et al. disclose the width of the embedded interconnection slot does not exceed 0.4 μm (less than 0.5 μm).

2. Claims 21 – 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Edelstein et al. (PN 6,181,012) in view of Nogami et al. (PN 6,242,349) and further in view of Maekawa (PN 6,171,957, of record).

Edelstein et al. and Nogami et al. disclose all of the claimed limitations except the metal film is formed by sputtering using a target wherein the purity of copper is not less than 99.999%.

However, Maekawa discloses forming a metal film (5) by sputtering using a target wherein the purity of copper is not less than 99.999%. Note Figures 1(a) – 2. Therefore, it would have been

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obvious to one of ordinary skill in the art at the time the invention was made to form the metal film of Edelstein et al. and Nogami et al. by sputtering using a target wherein the purity of copper is not less than 99.999%, such as taught by Maekawa in order to reduce the resistance of the metal film.

With regard to claims 21 and 23, Edelstein et al., Nogami et al. and Maekawa disclose the copper having purity of 99.999 wt% or higher. Edelstein et al., Nogami et al. and Maekawa do not disclose the copper having purity of 99.9999 wt%. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to form the copper having purity of 99.9999 wt% in order to produce the small line width and to increase the speed of the device to meet the performance goal.

3. Claims 24-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Edelstein et al. (PN 6,181,012) in view of Nogami et al. (PN 6,242,349) and further in view of Lai et al. (PN 6,136,680).

Edelstein et al. and Nogami et al. disclose the metal film is planarized by chemical mechanical polishing. Edelstein et al. and Nogami et al. do not disclose the first main surface of the semiconductor substrate is plasma treated in an atmosphere of a gas having reducing properties prior to forming a cap insulating film. However, Lai et al. discloses forming a metal film (30) is planarized by chemical mechanical polishing and a first main surface of the semiconductor substrate is plasma treated in an atmosphere of a gas having reducing properties prior to forming a cap insulating film (32). Note Figure 6 and Col. 7, line 15 – Col. 9, line 15. Therefore, it

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would have been obvious to one having ordinary skill in the art at the time the invention was made to plasma treat the first main surface of the semiconductor substrate of Edelstein et al. and Nogami et al. in an atmosphere of a gas having reducing properties prior to forming a cap insulating film in order to suppress hillocks formation.

With regard to claims 25-27, Edelstein et al., Nogami et al. et and Lai al. disclose the gas atmosphere comprises hydrogen (ammonia) and/or nitride hydride as its principal component element.

Response to Arguments

4. Applicant's arguments with respect to claim 20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

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CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

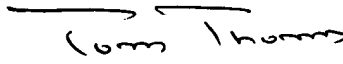
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hung K. Vu whose telephone number is (703) 308-4079. The examiner can normally be reached on Mon-Thurs 7:00-5:30, Eastern Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Vu

November 15, 2002


TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800